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13. ABSTRACT (Maximum 200 words)

The main goal of Stony Brook work will be to move as fast as possible toward the demonstration of first practical crested barriers based on a combination of plasma-grown Al2O3 layers with either thermally-grown aluminum oxide or silicon dioxide (see Fig. 7 and its discussion above). Listed below are the most urgent steps we plan to make in this direction:

1. Ways to combine plasma-formed (Cr19-type) layers with thermally-oxidized (CrO5-type) layers will be explored. One possible way is to deposit a thin (~2-nm) aluminum layer on the thermally-grown oxide, and plasma-oxidize it thoroughly. If this way will not give a sufficiently smooth aluminum film (e.g., because of poor wetting), other methods of the second layer deposition will be studied.
2. Effects of higher oxygen exposure and post-annealing on Cr30-type layers will be studied. Either of these procedure (or their combination) may lead to films combining high barrier of annealed Cr12 layers with larger thickness.
3. Rapid post-annealing at higher temperatures (up to 500°C) of CrO5-type films will be explored, in order to increase the barrier height even further, while sustaining the barrier homogeneity and reproducibility.
4. Chemical and physical structure of various aluminum oxide layers and their interfaces will be understood in more detail using such methods as high-resolution TEM, scanning TEM contrast imaging, and energy-loss spectroscopy, all available through our collaboration with Dr. Yimei Zhu of the Brookhaven National Laboratory (at no cost for the AFOSR).

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Final Report

Crested Tunnel Barriers for Fast, Scalable, Nonvolatile Memories

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1. Objectives

The main objective of this project is the experimental demonstration of the theoretically predicted enhanced quantum-mechanical tunneling through layered ("crested") barriers. If demonstrated in silicon-compatible materials with sufficient endurance under electric stress, this effect may enable high-density, high-speed nonvolatile memories that may potentially replace DRAM as the main random access memories of semiconductor electronics. With that objective, we have combined the expertise at Stony Brook University in crested barrier theory (Prof. Konstantin Likharev) and aluminum oxide layer growth (Prof. James Lukens) with that of Yale University (Prof. T.P. Ma and Dr. X. Wang) in jet vapor deposition of silicon nitride and silicon dioxide films, as well as in nonvolatile memory technology. The main results of our initial, 30-months effort are listed below.

2. First Stage Results

(i) Jet Vapor Deposition (Yale)

During the first year of this research project, we demonstrated successful deposition of SiO_2 and Si_3N_4 films by the JVD method, and Al_2O_3 films by thermal oxidation of deposited Al. We measured the electrical properties of these films, and obtained very promising results. However, we encountered a major problem in I - V characteristics of our synthesized Si_3N_4 and Al_2O_3 films; i.e., an area factor of many orders of magnitude was required in the theory to quantitatively fit the experimental data. Alternatively, the I - V data could be fit perfectly with a theoretical model, which required insertion of a thin but high barrier in between the electrode and the synthesized dielectric film. This mysterious phenomenon had existed and puzzled us for a long time until recently. Because the mismatch between the experimental data and the theory was later found to exist not only for MOS structures with synthesized dielectric films but also for those with thermal SiO_2 (although the degree of mismatch was less), it is likely that the problem may have arisen from several process steps besides film deposition, including, for example, possible formation of a thin layer of aluminum oxide during thermal evaporation of Al electrode. Study along this line has resulted in improved curve fitting of experimental data with theory, both on single-dielectric MOS structures such as $\text{Al}/\text{Si}_3\text{N}_4/\text{Si}$, and on one-side crested barrier structure consisting of $\text{Al}/(\text{Si}_3\text{N}_4/\text{SiO}_2)/\text{Si}$.

In the middle of this research, the JVD machine, which we used to deposit the aforementioned gate dielectrics, became unavailable to us because its owner (which loaned us the machine) decided to take it back. Therefore, we decided to design and construct our own deposition machine. After a year of diligent work, we had completed our own deposition machine, named the "MAD" (Molecular and Atomic Deposition) machine, and started to reproduce the gate dielectrics that we were able to get with the old JVD machine. At the present time, the quality of our MAD silicon nitride is even superior to our high-quality JVD nitride. In addition, with the MAD machine we can also produce HfO_2 with the quality comparable to, or even better than, the state-of-the-art ALD HfO_2 . As to be discussed in Sec. 3 below, HfO_2 could be a promising component in a crested barrier structure. Because of its higher dielectric constant and large conduction band offset with respect to SiO_2 , when a HfO_2 layer of appropriate thickness is combined with SiO_2 , the slope of such crested barrier will be steeper than that of a $\text{Si}_3\text{N}_4/\text{SiO}_2$ structure, projecting to significantly increased current injection efficiency or high I_H/I_L ratio, where I_H is high-field tunnel current and I_L is low-field tunnel current.

Figures 1 and 2 below are TEM of our nitrogen doped HfO_2 film (HfON herein) and the corresponding XPS profiles of film composition, respectively. Figure 3 shows multi-frequency C - V characteristics of an $\text{Al}/\text{HfON}/\text{Si}$ MOS structure with the HfON layer having an equivalent oxide thickness of 3 nm. Figure 4 shows the I - V characteristic of the same structure.

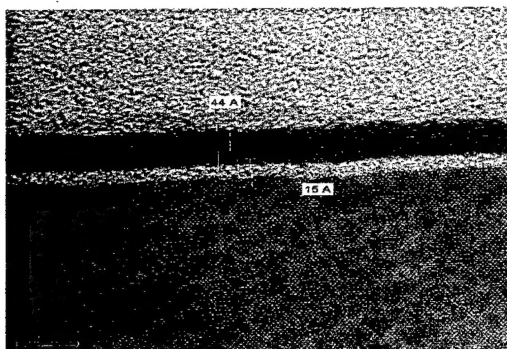


Fig. 1

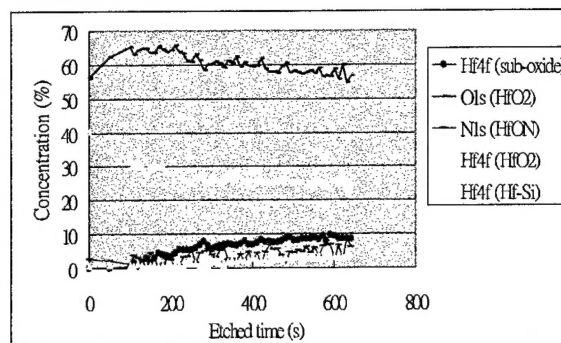


Fig. 2

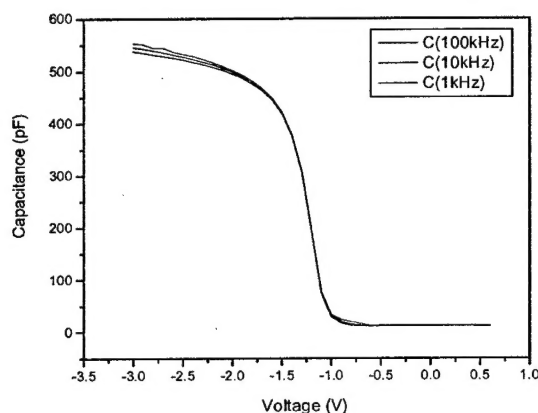


Fig.3

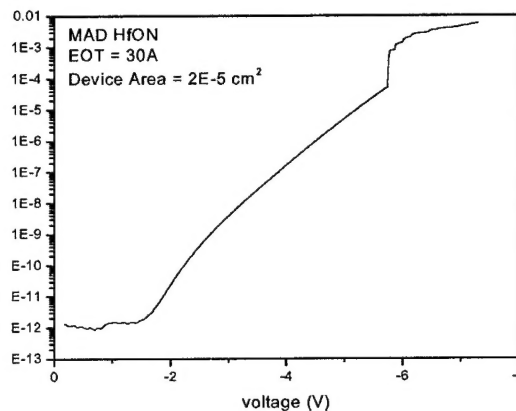


Fig. 4

(ii) AlO_x barriers (Stony Brook)

The goal of the Stony Brook effort was to evaluate aluminum oxidation techniques as a possible way to obtain high-quality Al_2O_3 layers for crested barriers. We have fabricated and tested several batches of aluminum oxide barrier samples, in order to evaluate parameters of such barriers grown in various oxidation modes. The barriers were parts of Nb-trilayer ($\text{Nb}/\text{Al}/\text{AlO}_x/\text{Nb}$) structures deposited on Si wafers.

For fabrication, a 150 nm Nb film was deposited by dc magnetron sputtering in a cryopumped system with the base pressure of 2×10^{-7} torr. This base electrode was covered by a similarly sputtered Al layer, 8 nm to 10 nm thick. This layer was then oxidized at room temperature in a static dry oxygen atmosphere in the pressure range from 1 to 100 torr for a time interval from 25 minutes to 40 hours to achieve the desired barrier transparency. After pumping down the chamber to the base pressure, a 150 nm Nb counter electrode was sputtered. Wafers were patterned by optical lithography with PMMA resist and reactive ion etching in SF_6 plasma. Each $5 \times 5 \text{ mm}^2$ chip had 18 tunnel junctions with sizes ranging from $3 \times 3 \mu\text{m}^2$ to $300 \times 300 \mu\text{m}^2$. After the junction etch, the PMMA etch mask was used as a mask to lift off a 150 nm SiO_2 dielectric layer insulating the base electrode from the wiring layer (the so-called self aligned lift-off process). Finally, a 300 nm Nb wiring layer was deposited and patterned using lift-off, with wiring configured to enable four-point measurements.

Tunnel barriers of both as-grown and post-annealed junctions were electrically characterized at room temperature and liquid helium temperatures using I - V measurements performed using a low-noise, highly sensitive setup. Measurements were done using sweeps of applied voltage with increasing amplitude until the hard breakdown.

Figures 5a and 5b show semi-log plots of the specific differential conductance $g \equiv A^{-1} dI/dV$ versus voltage V of thermally oxidized (TO) and plasma oxidized (PO) aluminum oxide layers at several selected annealing temperatures (solid symbols). One can easily see a

dramatic effect of the thermal annealing on the specific conductance of the TO- AlO_x , starting with annealing temperatures of 300°C. On the other hand, the annealing does not affect the conductance of the PO- AlO_x barriers much until $T_A \sim 450^\circ\text{C}$. Also, the breakdown voltage increases with the annealing temperature for both types of barriers: from $\sim 1\text{V}$ to $\sim 4\text{V}$ for TO- AlO_x , and from $\sim 4\text{V}$ to $\sim 5\text{V}$ for PO- AlO_x , but only at temperatures higher than 450°C.

In order to characterize the tunnel barrier change due to post-annealing, we have fitted the I - V curves with the results of "microscopic" theory of direct electron tunneling through a trapezoidally-shaped barrier. (The use of this theory is justified by the shape of the I - V curves and their weak temperature dependence, both indicative of the direct quantum tunneling as the main electrical transport mechanism.) The theory was based on the numerical joint solution of 1D Schrödinger and Poisson equations, with an approximate treatment of the inelastic electron scattering in the classically-allowed region of the barrier thickness.

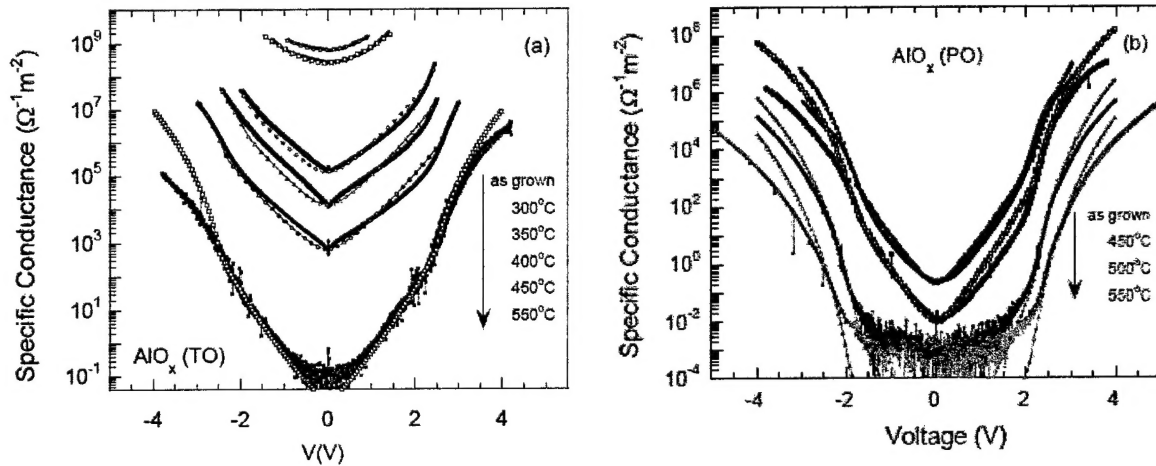


Fig. 5 Voltage V dependence of the specific dynamic conductance $g(V) \equiv A^{-1} dI(V)/dV$ (filled symbols) and its trapezoidal model fitting (open symbols) of post-annealed junctions with (a) thermally-grown and (b) plasma-grown barriers for various annealing temperatures (indicated inside each panel).

Figures 5 show the results of this fitting procedure, namely, the annealing temperature dependence of the best-fit values of three main barrier parameters. As had been expected from the raw I - V data, we have found that the annealing strongly affects the barrier profile of the TO- AlO_x , while leaving the one for the PO- AlO_x virtually unmodified. Namely, the barrier height of the TO- AlO_x is constant at $\sim 1.8\text{ eV}$ up to 300°C, but then starts to increase sharply, reaching $\sim 2.45\text{ eV}$ at 450°C. For even higher annealing temperatures, up to 550°C, the barrier height remains constant (within our error bars). By comparison, the average barrier height of PO- AlO_x is constant at $\sim 2.0\text{ eV}$ for all the annealing temperatures we have used. The observed increase of the average barrier height for TO- AlO_x is also correlated with an increase of the barrier thickness (see Fig. 5b), a $\sim 65\%$ increase in the breakdown electric field, and the reversal of the barrier asymmetry from negative to slightly positive. All these changes are consistent with the notion of substantial improvement of the uniformity and quality of the insulator, presumably as a result of structural modifications. Indeed, according to Ref. 5, the annealing of AlO_x above $\sim 300^\circ\text{C}$ leads to the gradual formation of the γ -phase Al_2O_3 from the initially amorphous low-temperature-grown aluminum oxide. It is interesting to notice in Fig. 5c that the effective thickness increases in a step-like pattern, with the step $\Delta d_{\text{eff}} \approx 0.6\text{ nm}$. For a realistic range of $m/m_0 = 0.35 \pm 0.20$, this corresponds to the physical thickness step of $\Delta d \approx 1.0 \pm 0.5\text{ nm}$, which is in the same ballpark as the lattice period 0.75 nm of the γ -phase Al_2O_3 . This means that each of the steps visible in Fig. 5c may correspond to an increase of the oxide layer thickness by one unit cell.

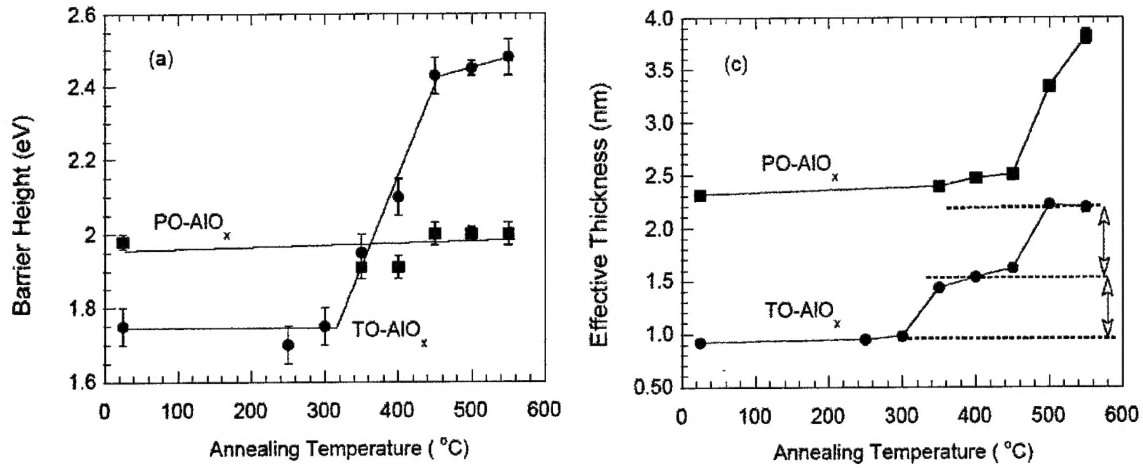


Fig. 6. Annealing temperature dependence of the three main fitting parameters: average barrier height $\Phi_a = (\Phi_B + \Phi_C)/2$, and the effective thickness $d_{eff} = (m/m_0)^{1/2}d$.

The above conclusions are not valid for PO-AIO_x, whose barrier height, barrier asymmetry, and thickness remain almost constant up to ~450°C. With the further increase of the annealing temperature, the barrier thickness increases sharply and the breakdown electric field decreases by at least 20% by 550°C, which indicates a sudden reduction of insulator quality. Putting a positive spin on this result, one can say that PO-AIO_x is stable relative to thermal processing at least up to 450°C. This is especially important for the fabrication compatibility with the CMOS process.

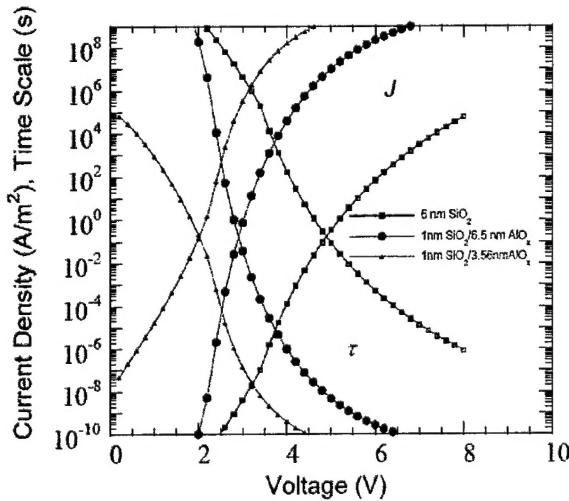


Fig. 7. Tunnel current density $J = I/A$ (increasing with the applied voltage V) and the recharging time constant $\tau \equiv C_0 V/J(V)$ (decreasing with voltage) for two layered tunnel barriers and one uniform SiO₂ barrier, calculated using the following parameters: $\Phi_a = 2.0$ eV, $m/m_0 = 0.5$ for the AlO_x layer and $\Phi_a = 3.34$ eV, $m/m_0 = 0.35$ for SiO₂. The used dielectric constant values are 10 and 3.9, respectively. The legend shows the physical thickness d of each layer.

Using the parameters found for the TO- and PO-AIO_x, we have carried out a theoretical evaluation of the best combination of CMOS-compatible materials, including aluminum oxides, for the fabrication of "crested barrier" tunnel junctions. Figure 7 shows our most promising prediction, results for a tunnel barrier comprised of a 1 nm-thick layer of SiO₂ and a 6.5-nm layer of PO-AIO_x. The plots show that such a barrier may combine a very short recharging time of ~1 nanosecond at $V = 5.5$ V, with a 10-year retention time at $V = 2$ V. Since this voltage ratio is below 3, the barriers may be the basis for nonvolatile random-access memories (NOVORAM) with very simple cell structure and matrix architecture.

To summarize, we have found that the barrier height of the thermally-grown oxide increases substantially, from 1.8 eV to 2.45 eV after annealing at 450°C, while the barrier height

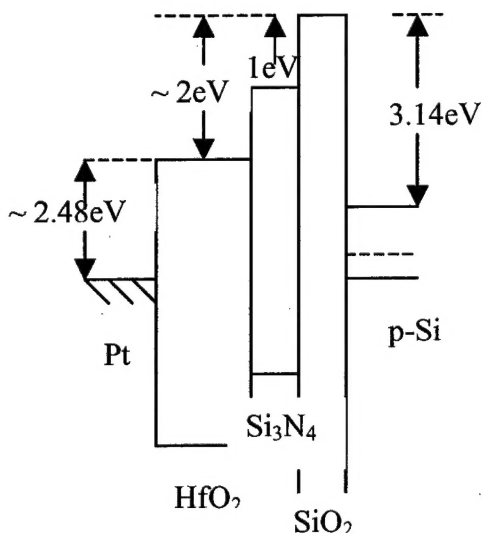
of the plasma-grown oxide remains constant at 2 eV for all temperatures. Calculations indicate that the plasma-grown oxide layers, in combination with a thin SiO₂ layer, are quite promising for crested barrier implementation.

3. Second Stage Research Plan

Encouraged by of Stage 1 results, we are going to pursue the following goal in our Stage 2 work.

(i) JVD Barriers (Yale)

Our plan for the immediate future is to realize a one-side graded crested barrier consisting of three dielectric layers shown in the diagram below. Also a platinum electrode is chosen to replace Al (used in our previous study) to achieve injection current control over a wide range of gate voltage. The role of Si₃N₄ layer sandwiched in between SiO₂ and HfO₂ is three-folds. Primarily, it blocks possible inter-mixing of elements in the HfO₂ layer and the SiO₂ layer. Secondly, its 1eV conduction band offset with respect to both SiO₂ (on its right) and HfO₂ (on its left) makes a graded barrier shape. Thirdly, the addition of the Si₃N₄ layer will definitely strengthen the dielectric breakdown of the crest barrier. To realize such a structure, the first thing we need to do is to figure out the appropriate thickness for each layer and the thickness ratios



between them by performing the simulation program developed at Stony Brook.

The next and very important step is to obtain good control of the thickness of each individual dielectric layer, to minimize the number of traps and to optimize the quality of interfaces, including SiO₂/Si interface and those between the three layers. Numerous C-V and I-V measurements, as well as curve fitting will be made over a wide range of temperatures to assure that our synthesized dielectrics have the right barrier heights as desired, and to understand the properties of the crested barriers. The results will provide very useful guide for the subsequent experiments. After such one-side crested tunnel barrier shows promising I_H/I_L ratio, we will seek to construct a double-side crested barrier to demonstrate the feasibility of the crested tunnel barrier concept.

(ii) Aluminum Oxide Barriers (Stony Brook)

The main goal of Stony Brook work will be to move as fast as possible toward the demonstration of first practical crested barriers based on a combination of plasma-grown Al₂O₃ layers with either thermally-grown aluminum oxide or silicon dioxide (see Fig. 7 and its discussion above). Listed below are the most urgent steps we plan to make in this direction:

1. Ways to combine plasma-formed (Cr19-type) layers with thermally-oxidized (Cr05-type) layers will be explored. One possible way is to deposit a thin (~2-nm) aluminum layer on the thermally-grown oxide, and plasma-oxidize it thoroughly. If this way will not give a sufficiently smooth aluminum film (e.g., because of poor wetting), other methods of the second layer deposition will be studied.

2. Effects of higher oxygen exposure and post-annealing on Cr30-type layers will be studied. Either of these procedure (or their combination) may lead to films combining high barrier of annealed Cr12 layers with larger thickness.

3. Rapid post-annealing at higher temperatures (up to 500°C ?) of Cr05-type films will be explored, in order to increase the barrier height even further, while sustaining the barrier homogeneity and reproducibility.

4. Chemical and physical structure of various aluminum oxide layers and their interfaces will be understood in more detail using such methods as high-resolution TEM, scanning TEM

contrast imaging, and energy-loss spectroscopy, all available through our collaboration with Dr. Yimei Zhu of the Brookhaven National Laboratory (at no cost for the AFOSR).

4. Reports and Publications

- [1] S. K. Tolpygo, E. Cimpoiasu, X. Liu, Yu. A. Polyakov, J. E. Lukens, and K. K. Likharev, "Tunneling Properties of Barriers in Nb/Al/AlO_x/Nb Junctions" *IEEE Trans. on Appl. Supercond*, vol. 13, pp. 99-102, Jun. 2003.
- [2] E. Cimpoiasu, S. K. Tolpygo, X. Liu, N. Simonian, Yu. A. Polyakov, J. E. Lukens, and K. K. Likharev, "Aluminum Oxide Layers as Potential Components for Crested Tunnel Barriers", report at the Electronic Materials Conference (2003).
- [3] E. Cimpoiasu, S. K. Tolpygo, X. Liu, Yu. A. Polyakov, N. Simonian, J. E. Lukens, and K. K. Likharev, "Tunneling Through Rapid Thermal Annealed Aluminum-oxide Layers", report at the APS March Meeting (2004).
- [4] E. Cimpoiasu, S. K. Tolpygo, X. Liu, Yu. A. Polyakov, J. E. Lukens, and K. K. Likharev, "Aluminum Oxide Layers as Possible Components for Layered Tunnel Barriers", *J. Appl. Phys*, submitted for publication.
- [5] E. Cimpoiasu, S. Tolpygo, X. Liu, and K. Likharev, "Effect of Rapid Thermal Annealing on Thin Aluminum Layer Oxides", *IEEE Electron. Dev. Lett*, submitted for publication.
- [6] R. Klie, Y. Zhu, E. Cimpoiasu, S. K. Tolpygo, and K. K. Likharev, "High Resolution Scanning Transmission Electron Microscopy Study of Thermally Annealed Thin Al₂O₃ Layers", paper in preparation.